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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/582,920

06/13/2006

Michinori Shinkai

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FITZPATRICK CELLA HARPER & SCINTO

1290 Avenue of the Americas

NEW YORK, NY 10104-3800

EXAMINER

TALBOT, BRIAN K

ART UNIT

PAPER NUMBER

1715

MAIL DATE

DELIVERY MODE

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/582,920	<b>Applicant(s)</b> SHINKAI ET AL.	
	<b>Examiner</b> Brian K. Talbot	<b>Art Unit</b> 1715	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 23-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 23-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

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1. The response filed 12/21/10 has been considered and entered. Claims 1-22 have been canceled. Claims 23-26 remain in the application.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
  1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claim Rejections - 35 USC § 103**

5. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furusawa et al. (7,285,305) (a) alone or (b) in combination with Lee et al. (2004/0045657).

Furusawa et al. (7,285,305) teaches a multilayered wiring board and method of producing the multilayered wiring board. Furusawa et al. (7,285,305) teaches polyamide insulating layers (22) between the wiring layers and an interlayer conducting post (18) for conducting between wiring pattern (17) and the wiring pattern (31) wherein the insulating layer is disposed around the conducting post (18) using a liquid drop discharge system (abstract). Looking at the Figs, conductive wirings (17) are formed with conductive posts (18) and then insulating layer is formed surround the posts (18). Then wiring layers (31) and posts (32) are formed that connect to the wiring layer (17) and insulating layer (33) is applied to surround the post (32).

Furusawa et al. (7,285,305) fails to teach first forming the insulating portion of the first layer and then the conductive layer but teaches the reverse of this process.

(a) While the Examiner acknowledges the fact that the claimed invention teaches process steps of forming the conductor and then insulator patterns as opposed to forming the insulator and then conductive patterns, it is the Examiner's position that one skilled in the art at the time the invention was made would have had a reasonable expectation of achieving similar success regardless of which layer was applied first and which layer was applied subsequently as long as both conductive and insulative layers are formed within the same layer as claimed.

(b) Lee et al. (2004/0045657) teaches method of forming a multilayer ceramic electronic device whereby a dielectric sheet with a pattern of via holes is formed on a conductive layer and

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subsequently the pattern of vias holes are filled with conductive paste (Figs. 1B-1D and Fig. 2).

The dielectric and conductive layers are formed by printing ([0004]).

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified Furusawa et al. (7,285,305) process by first forming the dielectric layer and then filling with conductor paste as opposed to forming conductor layer first and then dielectric layer surrounding the conductor as evidenced by Lee et al. (2004/0045657) with the expectation of achieving similar success, i.e. a layer including conductive and dielectric portions.

### **Response to Amendment**

6. Applicant's arguments with respect to claims 23-26 have been considered but are not found persuasive.

7. Applicant argued the prior art teaches forming a conductive layer first and then forming the insulating layer whereas the instant invention teaches forming the insulative layer first and then the conductive layer.

This has been addressed previously and noted above. Furthermore, regarding Lee et al. (2004/0045657), the reference teaches method of forming a multilayer ceramic electronic device whereby a dielectric sheet with a pattern of via holes is formed on a conductive layer and subsequently the pattern of vias holes are filled with conductive paste (Figs. 1B-1D and Fig. 2). The dielectric and conductive layers are formed by printing ([0004]). This dielectric sheet having holes therein would achieve the benefit argued by applicant and "allow precise

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application of the conductive material” and hence meets the claimed limitations as applied. It is the Examiner’s position that the benefits associated with the instant invention are achieved with the prior art as the dielectric layer is applied with openings for forming the conductive layer therein whether or no the multilayered structure had a conductive layer applied prior to alternating dielectric and conductive layers.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian K. Talbot whose telephone number is (571) 272-1428. The examiner can normally be reached on Monday-Friday 8AM-4PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian K Talbot/  
Primary Examiner, Art Unit 1715

BKT